

## Voltage regulator circuit arrangement

The invention relates to a voltage regulator circuit arrangement as defined in the preamble of claim 1.

The invention also relates to an integrated circuit comprising a voltage regulator circuit.

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Such voltage regulator circuit arrangements are commonly used, for example for generating supply voltages for micro-controllers and micro-processors. Different types and applications may require different supply voltage levels. In practice a wide variety of supply voltage levels exists.

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In practice a design of a voltage regulator circuit arrangement is used to obtain several output voltages. The output voltage generated by the voltage regulator circuit arrangement is adapted by changing component values of one or more components in the arrangement. In case the voltage regulator circuit arrangement is realized as an integrated circuit this implies that for a different output voltage a number of masks has to be modified. It may even be the case that a complete mask set has to be modified. Thus each output voltage requires a separate mask set, although the basic design of the voltage regulator circuit does not change. Furthermore due to the throughput time of IC processing this approach is rather inflexible.

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A known solution to overcome this disadvantage is a voltage regulator circuit arrangement having a number of programming inputs, each of which is either connected to a first reference voltage or to a second reference voltage, different from the first. Especially if the voltage regulator arrangement is designed as an integrated circuit this a disadvantage, since each programming input is an additional external input that requires an external pin and in general one would like to reduce the number of external pins as much as possible.

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Amongst others it is an object of the invention to provide a voltage regulator circuit arrangement with a reduced number of external terminals.

To this end the invention provides a voltage regulator circuit arrangement as defined in the opening paragraph which is characterized by the characterizing part of claim 1.

In this way the number of external terminals of the voltage regulator circuit arrangement is reduced. An advantage of the voltage regulator circuit arrangement according to the invention is that it is possible to change its output voltage by connecting a different sub-set of the plurality of internal terminals to the external terminal.

The above and other objects, features, and embodiments of the present invention will become more apparent from the following detailed description considered in connection with the accompanying drawings in which:

Fig. 1 shows a schematic diagram of a voltage regulator circuit arrangement according to the invention;

Fig. 2 shows a schematic diagram of an embodiment of the voltage regulator circuit arrangement according to the invention;

Fig. 3 shows a schematic diagram of another further embodiment of the voltage regulator circuit arrangement according to the invention;

Fig. 4 shows a schematic diagram of another further embodiment of the voltage regulator circuit arrangement according to the invention; and

Fig. 5 shows a schematic diagram of another further embodiment of the voltage regulator circuit according to the invention.

In these figures identical parts are in general identified with identical references.

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Fig. 1 shows a schematic diagram of a voltage regulator circuit arrangement according to the invention. The arrangement 100 comprises a voltage regulator 102 that in operation supplies an output voltage  $V_{out}$  at its output 104. The output voltage  $V_{out}$  is generated in dependence of a reference voltage  $V_{ref}$  supplied at its input. The reference voltage  $V_{ref}$  is generated by a reference voltage generation circuit 101. The reference voltage generation circuit has a plurality of inputs  $I_1, I_2, \dots, I_m$  which are connected to corresponding internal terminals  $T_1, T_2, \dots, T_m$ . A sub-set of the internal terminals  $T_1, T_2, \dots, T_m$  is connected to an external terminal 103.

In practice the voltage regulator 102, the reference signal generation circuit, and the internal terminals T1, T2, ..., Tm could be part of an integrated circuit whereby T1, T2, ..., Tm are bondpads of the integrated circuit. External terminal 103 could be a lead finger with in an integrated circuit package which is connected to an out side pin or contact area of the integrated circuit package. Only a sub-set of the internal terminals T1, T2, ..., Tm is connected to external terminal 103, thereby reducing the required number of external terminals and thus in practice reducing the required number of pins of an integrated circuit package. In the voltage regulator arrangement shown in Fig. 1 only internal terminal Tm is connected to external terminal 103, as is indicated by the continuous line between internal terminal Tm and external terminal 103. Possible connections between other internal terminals and external terminal 103 are indicated by broken lines. It will be clear that more than a number of internal terminal may be connected to external terminal 203 simultaneously. Conventionally such connections are made by means of bond-wires, but other known ways may also be used. The reference voltage Vref depends on which of the connectors T1, T2, ..., Tm is connected to external terminal 103 and a signal applied at external terminal 103.

Advantages of the invention are:

- just one mask set and one version on stock for the different output voltages.
- very small extra chip area (only bondpads).
- flexibility at the customer to change the output voltage some weeks before the delivering of the linear voltage regulators.
- possibility to change one metal-mask for more, not selectable on forehand, output voltage levels.
- fail Safe, as the output voltage is determined by the bondwires, and not by the customer.
- trimming can be very accurate at final testing as there is just one output voltage to trim; this is not possible if the selection is not done by bonding but externally in the application by pulling one or more pins to ground or to a higher voltage.

Fig. 2 shows a schematic diagram of an embodiment of the voltage regulator circuit arrangement according to the invention. The arrangement 200 comprises a voltage regulator 202 that in operation supplies an output voltage Vout at its output 204. The output voltage Vout is generated in dependence of a reference voltage Vref supplied at its input. The reference voltage Vref is generated by a reference voltage generation circuit 201. The reference voltage generation circuit has a plurality of inputs which are connected to corresponding internal terminals T1, T2, ..., Tm. A sub-set of the internal terminals T1, T2,

...,  $T_m$  is connected to an external terminal 203. In Fig. 2 only internal terminal  $T_{m-1}$  is connected to external terminal 203 as is indicated by the continuous line between internal terminal  $T_{m-1}$  and external terminal 203. Possible connections between other internal terminals and external terminal 203 are indicated by broken lines. It will be clear that a number of internal terminal may be connected to external terminal 203 simultaneously.

In the shown embodiment reference signal generation circuit 201 comprises a resistive ladder network. In the shown resistive ladder network a plurality of resistors  $R_1, R_2, \dots, R_{n-1}, R_n$  are connected in series. An electrode of the first resistor  $R_1$  is connected to a supply voltage or another pre-determined voltage. Another electrode of resistor  $R_1$  is connected to an intermediate node 210 that further is connected to internal terminal  $T_1$ , a second resistor  $R_2$ , and coupled to the input of the voltage regulator 202 for supplying the reference voltage  $V_{ref}$ . An electrode of the last resistor  $R_n$  is connected to internal terminal  $T_n$ . Another electrode of resistor  $R_n$  is connected an intermediate node 211 that is further connected to internal terminal  $T_{n-1}$  and an electrode of resistor  $R_{n-1}$ . Other internal terminals are connected to other intermediate nodes in the resistive ladder network.

By connecting a different internal terminal to external terminal 203 the voltage division ratio of the resistive ladder network will change, resulting in a different reference voltage  $V_{ref}$  being generated in response to the same input voltage provided at the external terminal 203. Alternatively a number of internal terminals may be connected to external terminal 203, thereby short-circuiting a part or parts of the resistive ladder network, resulting in the voltage division ratio to be changed. Depending on the application it may be advantageously that all resistors have the same value or that individual resistors have different values.

Fig. 3 shows a schematic diagram of another further embodiment of the voltage regulator circuit arrangement according to the invention. The arrangement 300 comprises a linear voltage regulator 302 that in operation supplies an output voltage  $V_{out}$  at its output node 315. The output voltage  $V_{out}$  is generated in a conventional way in dependence upon a first reference voltage  $V_{bg}$ , generated by a band-gap voltage reference circuit 301, supplied at a non-inverting input of the voltage regulator 302 and a second reference voltage  $V_{ref}$  supplied at an inverting input of the voltage regulator 302. The second reference voltage  $V_{ref}$  is generated by a reference voltage generation circuit comprising a resistive ladder network comprising a plurality of resistors  $R_1, R_2, R_3, R_4, R_5, R_6, \dots, R_n$  connected in series between node 315 and a node at a fixed voltage level, for instance ground. The resistive ladder network has a plurality of inputs formed by circuit nodes within

the resistive ladder network which are connected to corresponding internal terminals T1, T2, ..., Tm. A sub-set of the internal terminals T1, T2, ..., Tm is connected to an external terminal 303. In Fig. 3 only internal terminal Tm is connected to external terminal 303 as is indicated by the continuous line between internal terminal Tm and external terminal 303.

- 5 Possible connections between other internal terminals and external terminal 303 are indicated by broken lines. It will be clear that more than a number of internal terminal may be connected to external terminal 303 simultaneously. Conventionally such connections are made by for instance bond-wires.

In the resistive ladder network resistor R1 is connected between ground and  
10 node 310, which is further coupled to the inverting input of voltage regulator 302 for supplying the reference voltage Vref. Resistor R2 is connected between node 310 and node 311. Resistor R3 is connected between node 311 and node 312, which is further connected to internal terminal T1. Resistor R4 is connected between node 312 and node 313, which is further connected to internal terminal T2. Resistor R5 is connected between node 313 and  
15 node 314, which is further connected to internal terminal T3. Resistor R6 is connected to node 314 and via further resistors and nodes resistor coupled to resistor Rn. Resistor Rn, the last resistor in the resistive ladder network is connected to node 315, which is further connected to internal terminal Tm.

In Fig. 3 only internal terminal Tm is connected to external terminal 303 as is  
20 indicated by the continuous line between internal terminal Tm and external terminal 303. Possible connections between other internal terminals and external terminal 303 are indicated by broken lines. It will be clear that a number of internal terminal may be connected to external terminal 303 simultaneously.

By connecting additional internal terminal to external terminal 203 the voltage  
25 division ratio of the resistive ladder network will change, resulting in a different reference voltage Vref being generated in response to the same input voltage provided at the external terminal 303. Alternatively a number of internal terminals may be connected to external terminal 303, thereby short-circuiting a part or parts of the resistive ladder network, resulting in the voltage division ratio to be changed. Depending on the application it may be  
30 advantageously that all resistors have the same value or that individual resistors have different values.

In a typical application all elements shown in Fig. 3, except external terminal 303 are part of an integrated circuit located on a semiconductor material die. Internal terminals T1, ..., Tm are the terminals of the integrated circuit and are realized for instance in

the form of bond pads. In this application external terminal 303 is an internal terminal of an integrated circuit (IC) package, for instance a lead finger, which is connected to an external terminal of the IC package, for instance a connector in the form of a pin or another conventional electrical contact.

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$$V_{out} = V_{ref} * (R_{tot} / R_1), \text{ with}$$

$$R_{tot} = R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + \dots + R_n \quad (1)$$

- In conventional linear voltage regulators only bond-wire between bond-pad  
10    $T_m$  to the lead-finger 303 of the package has been mounted, resulting in a maximum output voltage  $V_{out,max}$  on the lead-finger 303 and therefore the corresponding pin of the package:

$$V_{out,max} = V_{ref} * (R_{tot,max} / R_1), \text{ with}$$

$$R_{tot,max} = R_1 + R_2 + R_3 + R_4 + R_5 + R_6 + \dots + R_n. \quad (2)$$

- When one of the extra bond-wires has been added from respectively bond-pad  
15    $T_3$ ,  $T_2$  or  $T_1$  to the lead-finger 303, a short has been made across the resistors  $R_6$  to  $R_n$ , or  $R_5$  and  $R_6$  to  $R_n$ , or  $R_4$ ,  $R_5$  and  $R_6$  to  $R_n$  respectively, resulting in a lower output voltage. The total resistor  $R_{tot}$  in formula (1) from  $V_o$  to ground will decrease to:  
 $R_1+R_2+R_3+R_4+R_5$ ,  $R_1+R_2+R_3+R_4$  and  $R_1+R_2+R_3$  respectively. The value of the resistors determines the different output voltages.

- 20                   The extra chip area is minimum: just the extra bond-pads. The number of bond-pads (three in this example) is not fixed to three, the minimum is one. Another advantage is that if the band-gap-voltage  $V_{bg}$  can be trimmed also the output-voltage can be trimmed very accurate at final-testing for that particular output voltage. The choice of the number and value of resistors depends on all expected output voltages, even if the voltage is  
25   not selected in the first IC. By changing one metal mask whereby the bond-pads  $T_3$ ,  $T_2$  and/or  $T_1$  are wired to another place in the resistor-bleeder new output voltages can be selected.

- Typical resistor values are:  $R_1=10k\Omega$ ,  $R_2=R_3=5k\Omega$ ,  $R_4=4k\Omega$ ,  
 $R_5=2.4k\Omega$  and the sum of  $R_6$  to  $R_m = 13.6k\Omega$ . This results, together with a bandgap-  
30   voltage of approx. 1.25V in the following possible output voltages:

5.0V (one bond-wire, only on bond-pad  $T_m$ ),

3.3V (bond-wires to bond-pad  $T_m$  and  $T_3$ ),

3.0V (bondwires to bondpad  $T_m$  and  $T_2$ ), and

2.5V (bondwires to bondpad  $T_m$  and  $T_1$ ).

Fig. 4 shows a schematic diagram of another further embodiment of the voltage regulator circuit arrangement according to the invention. The arrangement 400 is a modified version of the arrangement shown in Fig. 3. It comprises a linear voltage regulator 402 that in operation supplies an output voltage  $V_{out}$  at its output node 415. The output voltage  $V_{out}$  is generated in a conventional way in dependence upon a first reference voltage  $V_{bg}$ , generated by a band-gap voltage reference circuit 401, supplied at a non-inverting input of the voltage regulator 402 and a second reference voltage  $V_{ref}$  supplied at an inverting input of the voltage regulator 402. The second reference voltage  $V_{ref}$  is generated by a reference voltage generation circuit comprising a resistive ladder network comprising a plurality of resistors  $R_1, R_2, R_3, R_4, R_5, R_6, \dots, R_n$ , and  $R_a, R_b, R_c, R_d, R_e, R_f$ , and  $R_g$  connected between node 315 and a node at a fixed voltage level, for instance ground. The resistive ladder network has a plurality of inputs formed by circuit nodes within the resistive ladder network which are connected to corresponding internal terminals  $T_1, T_2, \dots, T_m$ . A sub-set of the internal terminals  $T_1, T_2, \dots, T_m$  is connected to an external terminal 403. In Fig. 4 only internal terminal  $T_m$  is connected to external terminal 403 as is indicated by the continuous line between internal terminal  $T_m$  and external terminal 403. Possible connections between other internal terminals and external terminal 403 are indicated by broken lines. It will be clear that more than a number of internal terminal may be connected to external terminal 403 simultaneously. Conventionally such connections are made by for instance bond-wires.

In the resistive ladder network resistor  $R_1$  is connected between ground and node 410, which is further coupled to the inverting input of voltage regulator 302 for supplying the reference voltage  $V_{ref}$ . Resistor  $R_2$  is connected between node 410 and node 411. Resistor  $R_3$  is connected between node 411 and node 412. Resistor  $R_4$  is connected between node 412 and node 413. Resistor  $R_5$  is connected between node 413 and node 414. Resistor  $R_6$  is connected to node 414 and via further resistors and nodes resistor coupled to resistor  $R_n$ . Resistor  $R_n$ , the last resistor in the resistive ladder network is connected to node 415, which is further connected to internal terminal 315. Resistor  $R_a$  is connected between node 412 and node 421. Resistor  $R_b$  is connected between node 412 and node 420. Resistor  $R_c$  is connected between node 414 and node 421. Resistor  $R_d$  is connected between node 414 and node 420. Resistor  $R_e$  is connected between node 420 and node 421. Resistor  $R_f$  is connected between node 415 and node 421. Resistor  $R_g$  is connected between node 415 and node 420. Internal terminal  $T_m$  is connected to node 415. Internal terminal  $T_2$  is connected to node 420. Internal terminal  $T_1$  is connected to node 421.

In Fig. 4 only internal terminal T<sub>m</sub> is connected to external terminal 403 as is indicated by the continuous line between internal terminal T<sub>m</sub> and external terminal 403. Possible connections between other internal terminals and external terminal 403 are indicated by broken lines. It will be clear that a number of internal terminal may be connected to external terminal 403 simultaneously.

In a typical application all elements shown in Fig. 4, except external terminal 403 are part of an integrated circuit located on a semiconductor material die. Internal terminals T<sub>1</sub>, ..., T<sub>m</sub> are the terminals of the integrated circuit and are realized for instance in the form of bond pads. In this application external terminal 403 is an internal terminal of an integrated circuit (IC) package, for instance a lead finger, which is connected to an external terminal of the IC package, for instance a connector in the form of a pin or another conventional electrical contact.

The advantage of the arrangement of Fig. 4 compared with the arrangement of Fig. 3 is that it possible to generate additional values of V<sub>out</sub> without introducing additional bond-pads. Alternatively one bond-pad less is required to generate four different output voltages. Typical resistor values are R<sub>1</sub>=10kOhm, R<sub>2</sub>=R<sub>3</sub>=0 Ohm, R<sub>4</sub>+R<sub>5</sub>=15kOhm, the sum of R<sub>6</sub> to R<sub>m</sub> = 30kOhm, R<sub>a</sub>=20kOhm, R<sub>b</sub>=R<sub>c</sub>=R<sub>e</sub>=infinite, R<sub>d</sub>=6kOhm, R<sub>f</sub>=130kOhm and R<sub>g</sub>=84kOhm. This results, together with a band-gap voltage of approximately 1.25V in the following possible output voltages:

- 5.00V (one bond-wire, only on bond-pad T<sub>m</sub>),
- 3.46V (bond-wires on bond-pad T<sub>m</sub> and T<sub>2</sub>),
- 2.88V (bond-wires on bond-pad T<sub>m</sub> and T<sub>1</sub>), and
- 2.50V (bond-wires to bond-pad T<sub>m</sub>, T<sub>2</sub> and T<sub>1</sub>).

Fig. 5 shows a schematic diagram of another further embodiment of the voltage regulator circuit according to the invention. The arrangement comprises a linear voltage regulator 502 that in operation supplies an output voltage V<sub>out</sub> at its output node 530. output node 530 is connected to an inverting input of linear voltage regulator 502. A controlled voltage source 503 generates a reference voltage V<sub>ref</sub> in dependence upon an digital output circuit generated by digital circuit 501. An output of a first comparator 510 is connected to a first input of digital circuit 502. An output of a second comparator 520 is connected to a second input of digital circuit 502. A non-inverting input of the first comparator 510 is connected to node 532. At an inverting input of the first comparator a first threshold voltage V<sub>th,h</sub> is provided. A non-inverting input of the second comparator 520 is connected to node 531. At an inverting input of the second comparator a second threshold



voltage  $V_{th,l}$  is provided. Node 532 is connected to an internal terminal Ta. Furthermore a current source 512, generating a first current  $I_h$ , is connected between node 532 and a node at a fixed voltage, for instance ground. Node 531 is connected to an internal terminal Tb. Furthermore a current source 522, generating a second current  $I_l$ , is connected between node 531 and a node at a fixed voltage, for instance ground. Node 530 is connected to internal terminal To.

In a typical application voltage regulator arrangement 500 is part of an integrated circuit, whereby internal terminals Ta, Tb, and To are the terminals of the IC, typically formed as bond-pads. The output voltage  $V_{out}$  of the output buffer, connected to the bondpad To, which is mounted to a corresponding lead finger of a package, will be equal to the selectable voltage  $V_{ref}$  of the voltage source 503. The voltage of the voltage source 503 depends on the signals provided at the outputs of the comparators 510 and 520.

If bond-pad Ta is not mounted via a bond-wire to the lead-finger of To, the input signal of comparator 510 is equal to the ground-level due to the current source  $I_h$ , resulting in a low level of the output signal of comparator 510. If bond-pad Ta is mounted via a bond-wire to the lead-finger of To, the input signal of comparator 510 is equal to  $V_{out}$ , and with a threshold of comparator 510 lower than the minimum selectable  $V_{out}$ , the output signal of comparator 510 is high.

If bond-pad Tb is not mounted via a bond-wire to the lead-finger of  $V_{out}$ , the input signal of comparator 520 is equal to the ground level due to the current source  $I_l$ , resulting in a low level of the output signal of comparator 520. If bondpad Tb is mounted via a bond-wire to the lead-finger of  $V_{out}$ , the input signal of comparator 520 is equal to  $V_{out}$ , and with a threshold of comparator 520 lower than the minimum selectable  $V_{out}$  signal, the output signal of comparator 520 is high.

With the output signals of the comparators 510 and 520 both depending on the presence or absence of the bond-wires from the lead-finger of the output voltage to the bond-pads Ta and Tb respectively, four different output levels can be selected. The levels  $V_{th,h}$  and  $V_{th,l}$  are lower than the minimum selectable output voltage. The reason is that during start-up of the voltage regulator, which is the ramping up of the output voltage  $V_o$ , the digital circuit has to decide on which level  $V_{out}$  will stop. If the two bond-pads are not mounted  $V_{out}$  stops at the minimum output voltage. If only bond-pad Ta is mounted,  $V_{out}$  stops at a value somewhat higher. If only bond-pad Tb is mounted,  $V_{out}$  stops at the value higher than the second one. If both bond-pads have been mounted,  $V_{out}$  ramps up to the maximum output voltage.

With the choice of these comparator levels,  $V_{out}$  will ramp-up smoothly, as it is already known during the ramp-up when  $V_{out}$  is nearly equal to the minimum selectable output voltage to what voltage  $V_{out}$  has to ramp up.  $V_{t,h}$  can be higher than  $V_{t,l}$ , but this is not needed.

5                   The digital circuitry can look continuously to the levels of the output signals of the comparators 510 and 520. Alternatively it can also decide to store the information once during the first ramping up of  $V_{out}$ . The advantage of the latter is that spikes on  $V_{out}$  will not influence the decision for the selected  $V_{out}$ , and that the current sources 512 and 522 and the comparators 510 and 520 can be switched off. This saves power supply current.

10                   Typically the currents  $I_l$  and  $I_h$  are in the range of 10-100 $\mu$ A. The thresholds  $V_{th,l}$  and  $V_{th,h}$  are in the range of 1-2V, and the selected output voltage  $V_{out}$  between 2V and 5V. The number of extra bond-pads ( $T_a$  and  $T_b$  in this example) is not fixed to two, it can be more or less, depending on the number of wanted selectable output voltages.

15                   The embodiments of the present invention described herein are intended to be taken in an illustrative and not a limiting sense. Various modifications may be made to these embodiments by those skilled in the art without departing from the scope of the present invention as defined in the appended claims.

20                   For instance in the above discussed embodiments the reference signal is a voltage domain signal. It will be clear to a skilled person that instead of a voltage domain signal a signal in for instance the current or charge domain could be used if a suitable reference generation circuit is provided.

25                   Furthermore although in the embodiments shown in Fig. 2, Fig. 3, and Fig. 4 resistive ladder networks are used to divide a signal provided at an external terminal, it will be clear that other kinds of voltage divider circuits may be applied equally well, or in case current or charge domain reference signals are to be generated, current, respectively charge divider circuits.

                  The voltage regulator circuit arrangement according to the invention can be used in applications whereby a range of power supply voltages are common, or as stand-alone product, or as part of a system in which one or more voltage regulators are integrated.